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PATENT & TRADEMARK OFFICE

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re patent application of:
Berthold et al.

MMB Docket No. **1890-0053**

Application No. **10/774,338**

Filed: **February 6, 2004**

For: **Method for a Parallel Production of an MOS Transistor and a Bipolar Transistor**

Examiner: **To be assigned**

Group Art Unit: **2812**

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on

September 9, 2004
(Date of deposit)

James D. Wood
Name of person mailing Document or fee

Signature

September 9, 2004
Date of Signature

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Pursuant to 37 CFR §1.56, Applicant hereby discloses the following references, copies of which are enclosed, regarding the above-identified patent application.

Patent References

U.S. Patent No.	Inventor	Issue Date
5,354,699	Ikeda et al.	October 11, 1994
5,641,692	Miwa et al.	June 24, 1997
5,824,560	Van Der Wel et al.	October 20, 1998
5,970,332	Pruijmboom et al.	October 19, 1999
6,001,676	Sawada, et al.	December 14, 1999
6,103,560	Suzuki	August 15, 2000

6,440,787 B1	Yoshihisa	August 27, 2002

Foreign Application	**Issue Date**	**Country**
JP 63-244768	October 12, 1988	Japan
JP 5-6961	January 14, 1993	Japan
WO 96/30940	October 3, 1996	PCT
WO 96/30941	October 3, 1996	PCT
EP 0 746 032 A2	December 4, 1996	Europe
EP 0 851 486 A1	January 7, 1998	Europe
JP 2001203288	July 27, 2001	Japan
JP 200040758	February 8, 2000	Japan

Articles

1) Widmann, Mader, Friedrich, "Technologie hochintegrierter Schaltungen", Springer Verlag, 1996.

The above-identified documents include those documents cited in the international examination procedure, including those cited in an International Preliminary Examination Report (English language copy enclosed) and International Search (copy enclosed), in a related PCT patent application number PCT/EP02/07313 filed on July 2, 2002, and prior art cited in the national examination of related applications. English translations of the Abstracts for JP 5-6961, JP 63-244768, and JP 2001203288 are also enclosed.

U.S. Patent No. 6,103,560 claims priority to EP 0 851 486 and may provide additional information.

U.S. Patent No. 5,824,560 claims priority to WO 9630940 and may provide additional information.

U.S. Patent No. 5,970,332 claims priority to WO 9630941 and may provide additional information.

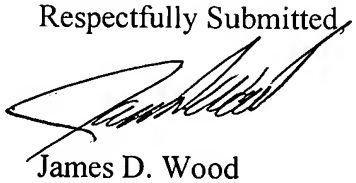
U.S. Patent No. 6,440,787 is an English language equivalent of JP 2001203288.

JP 200040758 discloses a method for producing MOS transistors and bipolar transistors. On a surface of a silicon substrate, electrodes are structured in a MOS region and electrodes are structured in a bipolar region. Sidewalls are generated at lateral surfaces of the structured electrodes which are subsequently removed in order to perform a doping of the drain and source portions.

"Technologie hochintegrierter Schaltungen", Widmann, Mader, Friedrich, Springer Verlag, 1996 discloses a BICMOS-process wherein a substrate is doped by iron implantation in order to produce conductive regions in the substrate. A silicon layer is produced after doping the substrate whereon an Si_3N_4 material is deposited on the silicon oxide layer. The Si_3N_4 layer is etched in order to allow a local oxidation whereafter the layer is removed. Collector terminals are produced by iron implantation via a structured photo resist layer. The photo resist layer is removed and a second photolithographic process using a second mask is performed in order to define the base zone of the bipolar transistors. The second photo resist layer is removed and a gate oxide is generated for the MOS transistors. A polysilicon gate layer is deposited and a further mask is used in order to define the gate. The source and drain regions are doped by iron implantation whereeafter an isolating oxide layer is generated in order to produce the dielectric layer of a capacitor. A second polysilicon layer is deposited for generating of the capacitor and high resistance resistors. The second polysilicon layer is etched to structure this polysilicon layer and a silicon oxide etching is performed in order to generate contact holes. A metal is deposited and etched in order to contact active regions of the device.

It is believed that no fees are due for the consideration of this Information Disclosure Statement. However, the Commissioner is hereby authorized to charge any deficiency or to credit any overpayment to Deposit Account No. 13-0014, but not to include any payment of issue fees.

Respectfully Submitted,



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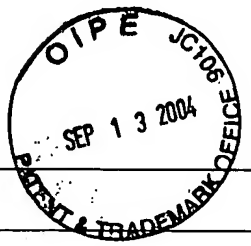
FORM PTO-1449 INFORMATION DISCLOSURE STATEMENT	MMB DOCKET NO. 1890-0053	APPLICATION NO.: 10/774,338
	APPLICANT(S): Berthold et al.	
	FILING DATE: February 6, 2004	GROUP ART UNIT: 2812



U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA	5,354,699	October 11, 1994	Ikeda et al.			
	AB	5,641,692	June 24, 1997	Miwa et al.			
	AC	5,824,560	October 20, 1998	Van Der Wel et al.			
	AD	5,970,332	October 19, 1999	Pruijmboom et al.			
	AE	6,001,676	December 14, 1999	Sawada et al.			
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	AG	6,440,787 B1	August 27, 2002	Yoshihisa			
	AH						
	AI						
	AJ						
	AK						

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AL	JP 5-6961	January 14, 1993	Japan			Yes No
	AM	JP 63-244768	October 12, 1988	Japan			Yes No
	AN	EP 0 746 032 A2	December 4, 1996	Europe			Yes No
	AO	JP 2001203288	July 27, 2001	Japan			Yes No
	AP	JP 200040758	February 8, 2000	Japan			Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AQ	1	Widmann, Mader, Friedrich, "Technologie hochintegrierter Schaltungen", Springer Verlag, 1996).
	AR	1	
	AS	1	

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicants.

FORM PTO-1449 INFORMATION DISCLOSURE STATEMENT	MMB DOCKET NO. 1890-0053	APPLICATION NO.: 10/774,338
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EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	BA						
	BB						
	BC						
	BD						
	BE						
	BF						
	BG						
	BH						
	BI						
	BJ						
	BK						

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	BL	WO 96/30940	10/03/1996	PCT			Yes No
	BM	WO 96/30941	10/03/1996	PCT			Yes No
	BN	EP 0 851 486 A1	01/07/1998	Europe			Yes No
	BO						Yes No
	BP						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AQ	2	
	AR	2	
	AS	2	

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